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09/988,208	11/19/2001	Kazuyuki Ohhashi	P21699	8111

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EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/988,208	OHHASHI, KAZUYUKI	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 6/12/2007 have been fully considered but they are not persuasive.

Applicant's Argument(s): Regarding independent claims 25, 26, 28, and 32, pages 6-8, the applicant argues that the claimed invention is not rendered obvious under 35 U.S.C. 103 over Sato, in view of the instant application's disclosed prior art and Omori for multiple reasons comprising:

(1) In contrast to the combinations recited in claims 25, 26, 28 and 32, Applicant's "Background of the Invention" section describes that amplitude adjustment is conventionally performed before phase control, and this feature is shown in Figure 4B of Applicant's disclosed prior art. However, according to the rejections of claims 25, 26, 28 and 32, Applicant's disclosed prior art would somehow lead one of ordinary skill in the art to adjust amplitude after sign inversion to obtain a first phase offset, though Applicant's disclosed prior art teaches specifically that amplitude adjustment is conventionally performed before phase control.

(2) Also in contrast to the combinations recited in claims 25, 26, 28 and 32, OMORI discloses, at column 2, lines 44-55, that a sign of a signal "is inverted without changing the value" of the quadrature component when the value shown in FIG. 4C of OMORI changes within either of two specified ranges. However, as should be clear

from OMORI, the sign inversion is not performed to obtain a first phase offset of a multiple of 90° in either of the specified ranges.

(3) Further, according to OMORI, any resultant phase offsetting occurs before amplitude adjustment. However, according to the rejections of claims 25, 26, 28 and 32, OMORI would somehow lead one of ordinary skill in the art to phase offsetting by a second phase offset smaller than 90° after amplitude adjustment. That is, the rejection of claims 25, 26, 28 and 32 is based on a proposal in the Office Action to place an amplitude adjuster between two stages of phase offsetting, though no such teaching is found anywhere in Applicant's disclosed prior art or the documents applied in the Office Action.

(4) As previously explained during prosecution, it would not be obvious to place an amplitude multiplier between phase shifter 201 in SATO and phase shifter 202 in SATO. Rather, as described in Applicant's "Background of the Invention" section, amplitude adjustment is conventionally performed before phase control, and this feature is shown in Figure 4B of Applicant's disclosed prior art. Accordingly, even the modification of SATO with the Admitted. Prior Art shown in FIG. 4B would result in the amplitude adjustment circuit being placed before phase shifter 201 and phase shifter 202 in SATO, and not between phase shifter 201 and phase shifter 202 in SATO.

(5) Further, there is no proper explanation for modifying SATO with the teachings of OMORI, let alone in the manner proposed in the Office Action. Rather, SATO and OMORI are directed to different and apparently incompatible proposals. That is, SATO is directed to processing both I and Q components of a signal, whereas OMORI is

directed to intentionally reducing processing when possible and not changing a Q component when changing an I component.

(6) Additionally, each of independent claim 28 and new independent claim 33 recite features of controlling the second phase offsetting based on a signal from a remote source (in claim 28 "a message included in a reception signal from a receiver that receives communication signals" from the claimed CDMA transmission apparatus). In contrast, SATO discloses, at col. 5, lines 37-52 (including Table II), that the second phase shifter 202 performs the second phase shifting operation according to the even-odd discrimination clock signal CLK3, which is not a "control signal from a remote source" as recited in claim 33 or the related features recited in claim 28. Further, it would not be obvious to modify SATO to control the second phase shifting based on a control signal from a remote source, as such a modification to SATO would render moot substantially all of the teachings of SATO relating to controlling the second phase shifting using CLK3.

Examiner's Response: In response to the argument set forth above, the examiner respectfully disagrees with the applicant because Sato discloses a phase offset calculator/ signal point mapper in a transmitter comprising a sign inverter that inverts a sign of signed binary data to obtain a first phase offset of multiple of 90 degrees (Fig. 1, block 201); and a phase offsetter that provides a second phase offset smaller than 90 degrees to a signal output from the sign inverter (Fig. 1, block 202). Sato is silent about placing an amplitude adjuster between the sign inverter and the phase offsetter. The instant application's disclosed prior art discloses a transmitter that

includes a phase offset calculator/ signal point mapper within the transmitter comprising an amplitude adjuster that is connected to the phase offsetter (Fig. 4B, blocks 406 and 407), wherein the input to the amplitude adjuster is **SRI** and **SRQ** which are phase offset calculation intermediate components (comparing figure 4B to figure 4A that is directed to embodiment of the present invention it reveals that the inputs to the amplitude adjuster of figure 4A is the same as the inputs to the amplitude adjuster of figure 4B that is labled as prior art) and the output of the amplitude adjuster 407 of figure 4B (AI and QI) is inputted to the phase offsetter 407 in figure 4B. And also, the instant application's discloses prior art discloses that adjusting/ controlling amplitude of the signal is necessary to compensate for amplitude variations of the signal in the transmitter is well known in the art (Pg. 2, lines 23-26). One of ordinary skill in the art would be motivated to include an amplitude adjuster prior to the phase offsetter circuitry in order to compensate for the amplitude variations of the signal. On the other hand, Omori discloses a transmitter that includes a sign inverter connected to an amplitude adjuster, wherein the amplitude adjuster is placed after the sign inverter in order to obtain a desired signal (Fig. 3; Col. 2, lines 44-64). One of ordinary skill in the art would be motivated to adjust the amplitude of the signal outputted from the sign inverter in order to obtain a desired modulated signal by compensating for the amplitude variations of the signal.

In response to arguments (1) to (3) and (5), the examiner would like to direct the applicant's attention to the fact that rejection is meant to be considered as a whole (e.g. the combination of the three references used in rejecting claims 25, 26, and 28). And

also, see the analysis cited above. The instant application's disclosed prior art is cited to show that the amplitude adjustment could be placed prior to phase offsetter. Omori is citer to show that amplitude adjustment could be placed after the sign inversion.

In response to argument (4), the examiner disagrees with the applicant because the modification of SATO with the Admitted. Prior Art shown in FIG. 4B would result in the amplitude adjustment circuit being **either** placed before phase shifter 201 and phase shifter 202 in SATO, **or** between phase shifter 201 and phase shifter 202 in SATO. However, comparing figure 4B to figure 4A that is directed to embodiment of the present invention it reveals that the inputs to the amplitude adjuster of figure 4A is the same as the inputs to the amplitude adjuster of figure 4B that is labled as prior art) and the output of the amplitude adjuster 407 of figure 4B (AI and QI) is inputted to the phase offsetter 407 in figure 4B; therefore, the amplitude adjuster is placed right before the phase offsetter.

In response to argument (6), the independent claim 28, does not recite features of controlling the second phase offsetting based on a signal from a remote source rather it recites a transmission controller that provides control information to the **signal point mapper** , wherein the signal point mapper includes a sign inverter, an amplitude adjuster, and a phase offsetter based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus. On the other hand, the independent claim 33 does recite the features of controlling the second phase offsetting based on a signal from a remote source. Sato is silent about controlling the second phase offsetting based on a signal from a remote source. The

instant application's disclosed prior art discloses that it is known to control the phase and amplitude of a transmission signal based on a message included in feedback information sent from a remote source (Pg. 1, lines 22-28) in order to improves transmission reliability. Therefore, one of ordinary skill in the art would be motivated to modify Sato's transmission system to operate in accordance with the closed loop transmission diversity mode as taught by the instant application's disclosed prior art in order to more accurately performing phase offsetting and consequently improving transmission reliability.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato, further in view of the instant application's disclosed prior art and Omori (US 6,239,666).

As to claim 25, Sato teaches a phase offset calculator (Fig. 1, means 102, 201; Fig. 2, means 201, 302, and 303) comprising a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90°; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal

output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. The instant application's disclosed prior art teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components prior to the phase-offsetter (Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver. Additionally, Omori discloses a modulator that uses a sign inversion circuit to invert the sign of the input signed binary data and adjusts the amplitude of the sign inverted signal (Fig. 3, means 31 and 36; Col. 2, Lines 29-64). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Omori with Sato and the instant application's disclosed prior art in order to obtain a desired transmission signal by compensating for the amplitude variations of the signal utilizing an amplitude adjuster (Col. 1, Lines 32-36; Col. 2, Lines 56-64).

As to claim 26, Sato discloses a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90°; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about

when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. The instant application's disclosed prior art teaches amplitude adjustment circuit that adjusts the amplitude of the phase offset signal before the phase-offsetter (Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver. Additionally, Omori discloses a modulator that uses a sign inversion circuit to invert the sign of the input signed binary data and adjusts the amplitude of the sign inverted signal (Fig. 3, means 31 and 36; Col. 2, Lines 29-64). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Omori with Sato and the instant application's disclosed prior art in order to obtain a desired transmission signal by compensating for the amplitude variations of the signal utilizing an amplitude adjuster (Col. 1, Lines 32-36; Col. 2, Lines 56-64).

As to claim 27, Sato further discloses that a fixed phase offset circuitry provides a predetermined amount of a fixed phase offset (Fig. 1, means 108), wherein said fixed phase offset circuitry controls a total phase offset amount with the phase offset implemented by the sign inverter to become a desired offset amount (Col. 4, Lines 44-67, Table I; Col. 5, Lines 37-60, Table II, means 202).

As to claim 28, Sato teaches a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed

binary data to a phase offset Θ of multiple 90°; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment; and a transmission controller that provides control information to the signal point mapper based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus. The instant application's disclosed prior art teaches amplitude adjustment circuit that adjusts the amplitude of the phase offset signal before the phase-offsetter (Fig. 4B, means 406 and 407); and a transmission controller that provides control information to the signal point mapper based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus (Pg. 1, Lines 16-28; Pg. 2, Lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal and clearly distinguish between interference signals from other mobile stations and the original reception signal (Pg. 2, Lines 1-5). Additionally, Omori discloses a modulator that uses a sign inversion circuit to invert the sign of the input signed binary data and adjusts the amplitude of the sign inverted signal (Fig. 3, means 31 and 36; Col. 2, Lines 29-64). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Omori with Sato and the instant application's disclosed prior

art in order to obtain a desired transmission signal by compensating for the amplitude variations of the signal utilizing an amplitude adjuster (Col. 1, Lines 32-36; Col. 2, Lines 56-64).

As to claim 29, Sato further discloses that a fixed phase offset circuitry that provides a predetermined amount of a fixed phase offset (Col. 4, Lines 44-67, Table I; Col. 5, Lines 37-60, Table II, means 202).

As to claims 30-31, the instant application's disclosed prior art further discloses that the phase and amplitude can be controlled for every transmit channel (Pg. 1, Lines 16-28; Pg. 2, Lines 12-20).

As to claim 32, Sato teaches a phase offset calculator (Fig. 1, means 102, 201; Fig. 2, means 201, 302, and 303) comprising a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90°; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. The instant application's disclosed prior art teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components prior to the phase-offsetter (Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates

for the amplitude variations of the signal to be received by the receiver. Additionally, Omori discloses a modulator that uses a sign inversion circuit to invert the sign of the input signed binary data and adjusts the amplitude of the sign inverted signal (Fig. 3, means 31 and 36; Col. 2, Lines 29-64). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Omori with Sato and the instant application's disclosed prior art in order to obtain a desired transmission signal by compensating for the amplitude variations of the signal utilizing an amplitude adjuster (Col. 1, Lines 32-36; Col. 2, Lines 56-64).

Claims 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato, further in view of the instant application's disclosed prior art.

As to claim 33, Sato teaches a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90°; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about controlling the phase offsetting based on a signal from a remote source. The instant application's disclosed prior art teaches a transmission controller that provides control information from a remote source to the phase offsetting circuit (Pg. 1, Lines 16-28; Pg. 2, Lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art to control the operation of the phase offsetting circuitry based on a control signal received from a remote source as taught by the instant application's disclosed prior art in order to

improve the level of a reception signal and clearly distinguish between interference signals from other mobile stations and the original reception signal (Pg. 2, Lines 1-5).

As to claim 34, Sato discloses providing the sign inverted signal to phase offsetter circuitry by using at least one switch (Fig. 2, means 301).

As to claim 35, the instant application's disclosed prior art further teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components prior to the phase-offsetter (Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver. Additionally, Omori discloses a modulator that uses a sign inversion circuit to invert the sign of the input signed binary data and adjusts the amplitude of the sign inverted signal (Fig. 3, means 31 and 36; Col. 2, Lines 29-64). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Omori with Sato and the instant application's disclosed prior art in order to obtain a desired transmission signal by compensating for the amplitude variations of the signal utilizing an amplitude adjuster (Col. 1, Lines 32-36; Col. 2, Lines 56-64).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is 571-272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Freshteh Aghdam
Examiner
Art Unit 2611

August 3, 2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER